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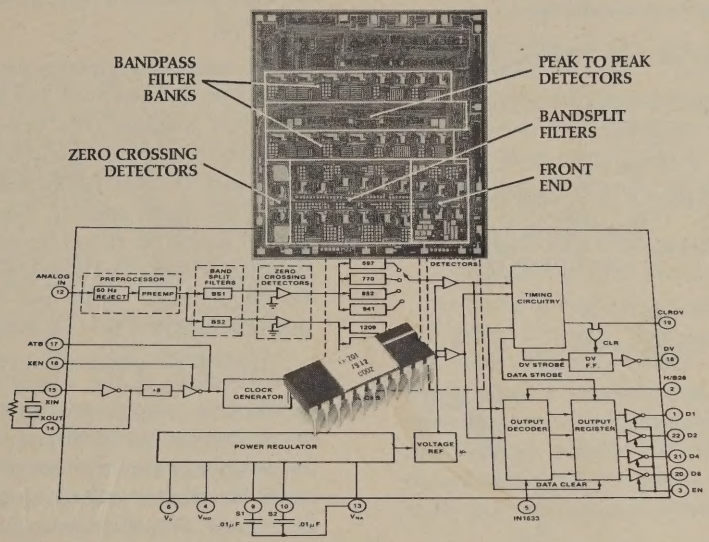
SSI 201
DTMF Receiver

Monolithic Dual-Tone Multi-frequency Receiver Application Note



The SSI 201 Integrated DTMF Receiver is a complete Touch-Tone® detection system. It operates in a stand-alone mode for the majority of telecommunications applications, thereby providing the most economical implementation of DTMF signaling systems possible. It combines precision active filters and analog circuits with control logic on a monolithic CMOS integrated circuit. Its use is straightforward and the external component requirements are minimal. This Application Note describes the system requirements and performance of the SSI 201 DTMF Receiver.

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Application Note
SSI 201 DTMF Receiver

I. HOW THE SSI 201 WORKS

General Description of Operation

The task of a DTMF receiver is to detect the presence of a valid tone pair on a telephone line or other transmission medium. What constitutes a valid tone pair? The following table gives the established Bell system standards:

One Low-Group Tone —and— One High-Group Tone	697 or 770 or 852 or 941 Hz 1209 or 1336 or 1477 or 1633 Hz
Frequency Tolerance	$f_o \pm (1.5\% + 2Hz)$
Amplitude Range	$-24dBm \leq A \leq +6dBm$ @ 600Ω
Relative Amplitude (Twist)	$-8dB \leq \frac{\text{High-Group Tone}}{\text{Low-Group Tone}} \leq +4dB$
Duration	40ms or longer
Inter-tone Pauses	40ms or longer

The presence of a valid tone pair indicates a single dialed digit; to generate a valid digit sequence, each tone pair must be separated by a valid pause. To achieve quality data reception, the DTMF receiver must faithfully identify all valid tone pairs and not mistakenly decode other signals as tone pairs.

Figure 1 is the SSI 201 block diagram. In general terms, the detection scheme is as follows: The analog input is pre-filtered and then split into two bands, each of which contains only one DTMF tone group. The output of each band-split filter is amplified and limited by a zero-crossing detector to produce a square wave at the dominant frequency present in that filter. Thus, if the only signal at the receiver input is a valid tone pair, the output of the high-group and low-group zero-crossing detectors are square waves at a high-group tone frequency and a low-group tone frequency, respectively. A bandpass filter group is driven by each zero-crossing detector; for a valid tone pair, one of the four low-group filters and one of the four high-group filters have a high output level. By level detecting the outputs of all eight bandpass filters, proper decoding of the tone pair is achieved.

In the telephone environment, speech and noise are often present on the line with the touch tones, compounding the detection problem. The SSI 201 architecture compensates for such interference providing talk off (speech immunity) and signal to noise performance surpassing that of available digital detection circuits. The key to this superiority is the use of bandstop filters to perform the band-split function (instead of the simpler and more common bandpass filters). In combination with the zero-crossing detectors, they provide excellent talk-off characteristics. Why is this so?

The function of the zero-crossing detectors (limiters) is to produce a square wave at the prime frequency emanating from the band-split filters. If a pure tone is not present, a rectangular wave with variable period will result. This is the case for voice or noise or whenever significant interference is present with the tones. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero-crossings shift. Eventually, no single bandpass filter pair will contain significant power long enough to result in a tone detection. To be most immune to false decodes—by far the worst type of DTMF receiver error—it makes sense to eliminate as little of the incoming audio spectrum as possible ahead of the limiters. Bandpass filters reject all signals except a tone group, while the SSI 201 bandstop filters reject only one tone group, retaining

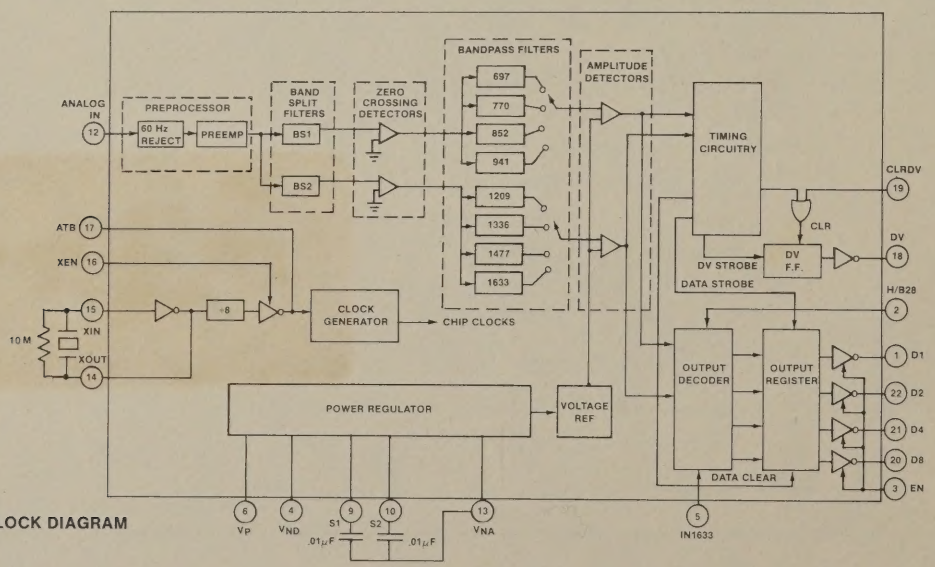


FIGURE 1. SSI 201 BLOCK DIAGRAM

the other tone group plus all other interfering audio energy. Thus it is more likely that the zero crossings will be skewed in the presence of interference with a bandstop front end than with a bandpass front end, making false tone detection far less likely.

Detailed Description of Operation

Preprocessor

The analog input first passes through the preprocessor which rejects 60 Hz and dial tone, and shapes the remaining spectrum. Dial tone and 60 Hz frequencies are attenuated to avoid filter overload which could prevent valid tone detection. In addition, the preprocessor emphasizes the higher part of the audio spectrum (typically attenuated by phone lines) to improve talk-off performance and attenuates signals above 6kHz to reduce the incoming signal to noise ratio requirement.

Bandstop Filters and Zero-Crossing Detectors

Driven by the preprocessor output, the bandstop filters separate the tone groups and drive the zero-crossing detectors. These detectors have very high gain and produce a constant amplitude output for signals above the minimum specified amplitude limits, and thus perform an AGC function. This makes detection independent of the amplitude of a valid tone pair. The SSI 201 discriminates on twist, or the relative amplitude of the two tones. This is accomplished by producing "floors" in the bandstop filters, so that a portion of the other tone group remains. Then, if the twist is too great, the zero crossings will be skewed enough by the opposite band tones to prevent detection.

Bandpass Filters and Amplitude Detectors

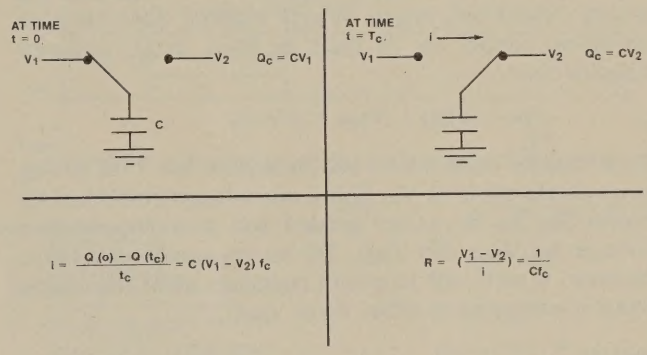
The bandpass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the filter output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuitry to ascertain the presence of one and only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

Timing and Logic

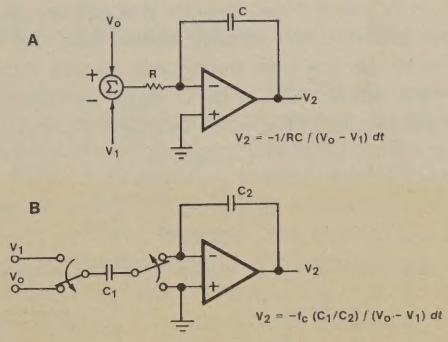
The only precision external element needed for the SSI 201 is a 3.58 MHz crystal for the on-board oscillator. This generates the precise clock for the filters and for the logical timing and controlling of the receiver. The SSI 201 is primarily analog in nature, so the logic performs bookkeeping, output formatting, and so on.

Circuit Implementation

The SSI 201 is an analog-digital system that is revolutionary in its incorporation of functions historically requiring combinations of passive and active discrete components, hybrids and digital ICs. For the first time, precision active filters with no external components or trimming requirements have been integrated with analog functional blocks and standard MOS logic. These are switched-capacitor filters* designed via classical techniques and implemented using switched capacitor resistors and integrators as shown in Figure 2. Because the filter characteristics, i.e. center frequency, Q, bandwidth and gain, are all defined by capacitor ratios, they are inherently very accurate and stable. The zero-crossing detectors and amplitude detectors are also precision analog circuits, and employ auto-zero techniques to null offsets contributed by the amplifiers and other circuitry. The logic is standard low-power, high noise immunity CMOS.



R from C. Switching a capacitor between two nodes simulates a resistor whose value depends only on the capacitor value and the switching frequency. This switched-capacitor technique allows the integration of precision filters on the DTMF chip.



Integrator. In a modification of standard integrator (**A**), C_1 of the differential switched-capacitor integrator (**B**) first charges to the difference between the two input voltages, then transfers the charge to C_2. The periodic transfer of charge appears as a current flow.

FIGURE 2. SWITCHED-CAPACITOR FILTERS

*G.M. Jacobs, G.F. Landsburg, B.J. White and D.A. Hodges, "Touch-Tone Decoder Chip Mates Analog Filters with Digital Logic," Electronics, Vol 52, No. 4, March 15, 1979, pp 105-112 (Reprints available from SSi).

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II. HOW TO USE THE SSI 201

Power Supply

The SSI 201 operates from 0°C to 70°C with a 12V ± 10% supply and typically draws 29mA. Excessive power supply noise should be avoided and to aid the user in this regard, power supply options are provided.

As with all active filter circuits, the SSI 201 is susceptible to excess power supply noise generating spurious signals at the filter outputs. In order to ensure reliable detection of -24dBm tones by the SSI 201, the wide-band power supply noise must be limited to less than 25mV peak-to-peak. Systems with higher minimum tone amplitudes will work properly with correspondingly higher power supply noise.

Since the digital circuitry of the SSI 201 possesses the high noise immunity characteristic of CMOS logic, limited power supply noise is required only for the analog supply (V_{NA}). Provision has been made on the SSI 201 to separate the analog (V_{NA}) and digital (V_{ND}) supplies, permitting an unfiltered supply to be used at V_{ND}. It is necessary however that:

$$V_{ND} < V_{NA} + .5 \text{ volts}$$

Power supply noise effects will be slightly less if the analog input is referenced to V_P. This is normally accomplished by connecting V_P to system ground and providing negative voltages for V_{NA} and V_{ND}. The power supply noise limit, however, is sufficient to ensure operation when the analog input is referenced to either V_P or V_{NA}.

Inputs

The SSI 201 contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if input or output voltages are not constrained to the range between V_P and V_{ND}.

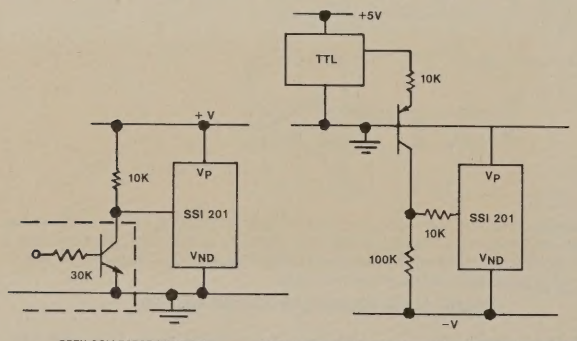


FIGURE 3. INTERFACE CIRCUITS FOR CONVERSION FROM TTL OUTPUT LEVELS TO SSI 201 INPUT LEVELS.

The digital inputs (H/B28, EN, IN1633, XEN and CLRDV) are directly compatible with standard CMOS logic parts powered by V_P and V_{ND}. Each input presents an impedance of greater than $10^9\Omega$ to incoming signals. To guarantee logic levels, inputs should swing to within 30% of V_P or V_{ND}. If it is desired to control the SSI 201 with TTL, the interface circuits shown in Figure 3 may be used.

The ANALOG IN input is the signal input pin to the SSI 201 receiver, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 4. The signal level at the ANALOG IN pin must neither exceed the positive supply nor fall more than 22V below it. If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a .01μF ± 20% capacitor. The internal bias resistor is greater than 100kΩ.

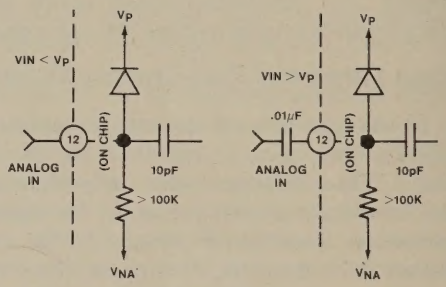


FIGURE 4. DIRECT AND AC COUPLED INPUT CONFIGURATIONS

The SSI 201 will tolerate total input rms noise up to 12dB below the lowest amplitude tone. For most telephony applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the SSI 201 unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter of Figure 5 may be employed to band limit the incoming signal.

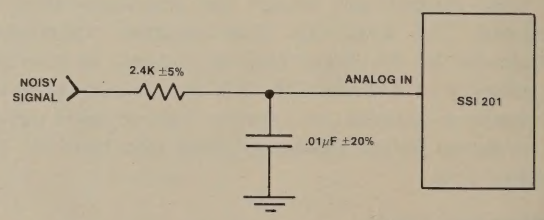


FIGURE 5. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT.

The S1 and S2 pins are connected to a portion of the zero-crossing detector circuitry. These pins should be bypassed to system ground with at least 0.01μF ± 20% capacitors.

Outputs

The digital outputs of the SSI 201 (D1, D2, D4, D8, DV, ATB) swing between V_P and V_{ND} and are fully compatible with standard CMOS logic parts powered from V_P and V_{ND}. The I-V characteristic of the digital outputs is plotted in Figure 6.

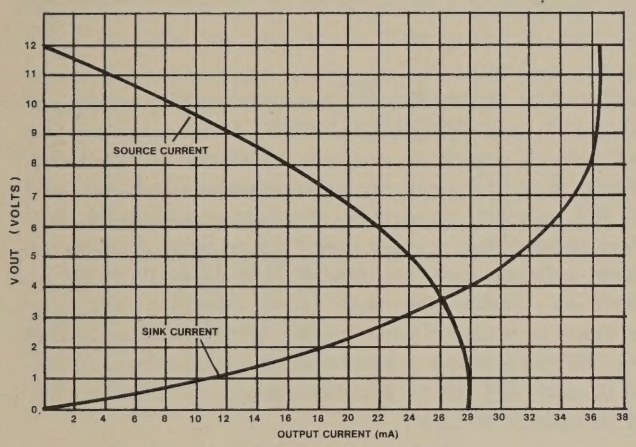


FIGURE 6. SSI 201 TYPICAL DATA OUTPUT ($V_P - V_{ND}$ = 12.0v)

A standard CMOS 4049B or 4050B can be used as shown in Figure 7 to interface the SSI 201 to TTL or low voltage MOS.

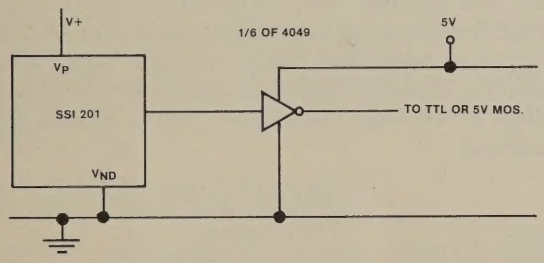


FIGURE 7. SSI 201 TO TTL OR LOW VOLTAGE MOS INTERFACE.

The data outputs (D1, D2, D4, D8) are three-state enabled to facilitate interface to a three-state bus. Figure 8 shows the equivalent circuit for the data outputs in the high impedance state. Care must be taken to prevent either diode in Figure 8 from becoming forward biased.

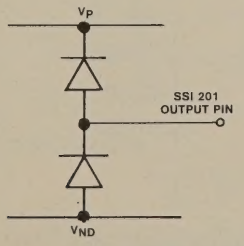
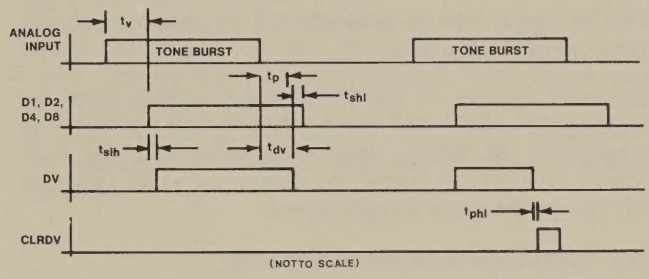


FIGURE 8. EQUIVALENT CIRCUIT OF SSI 201 DATA OUTPUT IN HIGH IMPEDANCE STATE

Timing

A timing diagram illustrating receiver operation is shown in Figure 9. Within 40ms of a valid tone pair appearing at the SSI 201 receiver input, the data outputs (D1, D2, D4, and D8) will become valid. Seven microseconds after the data outputs have become valid, DV will be raised. The data outputs will remain valid and DV will remain high as long as a valid tone pair is present at the receiver input. Within 40ms of the removal of a valid tone pair from the input, the SSI 201 will recognize a valid pause. DV is lowered approximately 45ms after the tone pair is removed. The data outputs will be cleared (all set to zero) 4.4ms after DV is lowered. The SSI 201 timing guarantees that the DV strobe will be of at least the same duration as the incoming tone pair. Figure 9 also lists the propagation delay specifications for the digital outputs of the SSI 201.



KEY

SYMBOL	DEFINITION	SPEC MIN	SPEC TYP	SPEC MAX	UNIT	CONDITION (V_P - (V_{NA} = V_{ND}) = 12V ±10% TA = 0°C-70°C
t_v	TONE DETECTION TIME	20	--	40	ms	--
t_{sih}	DATA OVERLAP OF DV RISING EDGE	7	--	--	μs	CLRDV = V_{ND}, EN = V_P
t_p	PAUSE DETECTION TIME	25	--	40	ms	--
t_{dv}	TIME BETWEEN END OF TONE AND FALL OF DV	40	45	50	ms	--
t_{shl}	DATA OVERLAP OF DV FALLING EDGE	4	--	4.4	ms	--
t_{phl}	PROP. DELAY: RISE OF CLRDV TO FALL OF DV MEASURED AT 50% POINTS	--	--	1	μs	Cl = 300 pF
---	OUTPUT ENABLE TIME: MEASURED FROM 50% POINT OF RISING EDGE OF EN TO THE 50% POINT OF THE DATA OUTPUT WITH RI TO OPPOSITE RAIL.	--	--	1	μs	Cl = 300pF, RI = 10K
---	OUTPUT DISABLE TIME: MEASURED FROM 50% POINT OF FALLING EDGE OF EN TO TIME AT WHICH OUTPUT HAS CHANGED 1V WITH RI TO OPPOSITE RAIL	--	--	1	μs	Cl = 300pF, RI = 1K ΔV = 1V
---	OUTPUT 10-90% TRANSITION TIME	--	--	1	μs	Cl = 300pF.

FIGURE 9. TIMING DIAGRAM AND SPECIFICATIONS.

Provision has been made on the SSI 201 for handshake interface with an outside monitoring system. In this mode, the DV strobe is polled by the monitoring system at least once every 40ms to determine whether a new valid tone pair has been detected. If DV is high indicating that a new valid tone pair has been detected, the monitoring system stores the coded data present at the data outputs of the receiver and clears DV by pulsing CLRDV high. With some systems operating in the handshake mode, it may be desirable to know when the valid tone has ended. Ordinarily this would be indicated by the falling edge of DV. However, in the handshake mode, DV is cleared by the monitoring system each time a new valid tone is detected and, therefore, cannot be used to determine when a valid tone pair has ended. The termination of a valid tone pair in this case may be observed by detecting the clearing of the data outputs. Since, in hexidecimal format (the mode

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normally used with a handshake interface), the all zero state represents a commonly unused tone pair (D), the end of a valid tone pair may be detected by connecting a four-input NOR gate to the outputs and sensing the all zero state.

Time Base

The SSI 201 contains an on-chip oscillator for a 3.579545 MHz parallel resonant quartz crystal. The CTS Part No. MP036 or Workman Part No. CY1-C or equivalent is recommended for use with the SSI 201 oscillator. The crystal is connected between XIN and XOUT, while XEN is tied high. In this mode, the ATB (alternate time base) pin delivers a square wave output at one-eighth the crystal oscillator frequency (447.443 kHz). A capacitor (C≅10pF) may be added in parallel with the crystal to trim the oscillator frequency, but is generally not required for proper operation of the SSI 201.

The ATB pin can be converted to a time base input by removing the crystal and tying XIN and XEN high and low respectively. By driving these ATB inputs with the ATB output of a crystal connected device, up to 25 receivers may be operated with a single crystal.

Dial Tone Rejection Requirements

The SSI 201 tolerates precise dial tone (350 Hz and 440 Hz at equal amplitudes) up to 0 dB relative to the lowest Touch-Tone® level*—adequate for most applications. In a high dial tone environment, the filter of Figure 10 may be used. This filter exhibits an elliptic highpass response that provides a minimum of 18 dB rejection at 350 Hz and 24 dB rejection at 440 Hz so long as the component tolerances indicated are observed. The SSI 201 on-chip filters reject 350 Hz at least 6 dB more than 440 Hz. Therefore, employing the filter of Figure 10 yields a dial tone tolerance of +24 dB. In a system where -24 dBm Touch-Tones® are present, the SSI 201 used in conjunction with the filter of Figure 10 will operate correctly in the presence of a 0 dBm dial tone (-3 dBm per dial tone frequency). The filter of Figure 10 also rejects 60 Hz by approximately 30 dB.

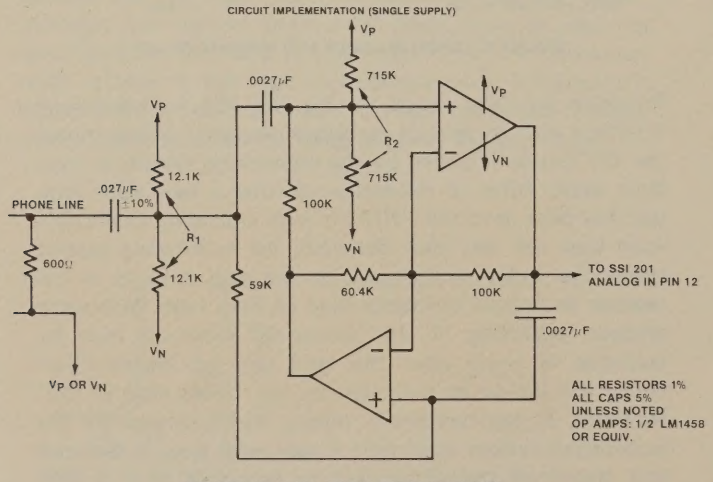

FIGURE 10. DIAL TONE REJECT FILTER.

*For dial tones of different amplitudes, the total power of the two dial tone frequencies must be no more than 0 dB relative to the lowest amplitude Touch-Tone.

The dial tone filter circuit is shown operated from the same single supply as the SSI 201 necessitating the splitting of resistors R_1 and R_2 for proper biasing of the op amps. If a dual polarity supply is available to power the op amps, resistors R_1 and R_2 may be replaced with single 5.9 kΩ and 357 kΩ resistors, respectively, connected to ground. It is recommended that the dial tone filter be powered from the highest voltage supply available (within the limits of the op amps) to provide the large signal handling capability necessary to accept Touch-Tones® in the presence of dial tone, 60 Hz, and any interference. Input coupling requirements to the SSI 201 must be observed as mentioned earlier in this application note.

III. PERFORMANCE DATA

The SSI 201 tone receiver has been subjected to the rigorous tests on the Mitel CM7290 tone receiver test cassette. This cassette checks receiver detection bandwidth, maximum acceptable amplitude ratio (twist), receiver guard time, dynamic range and signal to noise ratio. It also evaluates the receiver's speech immunity (talk-off) with a recording of excerpts from many hours of telephone conversations.

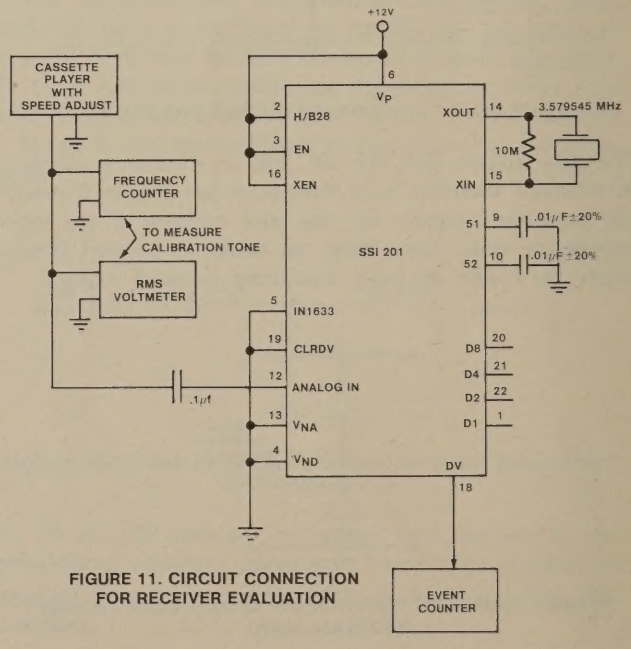

FIGURE 11. CIRCUIT CONNECTION FOR RECEIVER EVALUATION

The evaluation circuit shown in Figure 11 was used to characterize the SSI 201. The speed and output level of the tape deck must be adjusted so that the calibration tone at the beginning of the tape is at exactly 1000Hz and 2V rms.

Test results for the SSI 201 are summarized in Table I. The SSI 201 registers only two "hits" on the talk-off test-performance as good as the best receivers currently available. The SSI 201 detects all 1000 pulses in the 12 dB signal-to-noise ratio test unlike many tone receivers incorporating digital period counting algorithms. In short, the measured performance data demonstrates that the SSI 201 is a monolithic realization of a full "central office quality" DTMF receiver.

TABLE I
MITEL #CM7290 TAPE TEST RESULTS:
(Averaged for 10 parts)

TEST #	RESULTS
2a,b	B.W. = 5.0% of fo
2c,d	B.W. = 5.0% of fo
2e,f	B.W. = 5.3% of fo
2g,h	B.W. = 4.9% of fo
2i,j	B.W. = 5.0% of fo
2k,l	B.W. = 5.3% of fo
2m,n	B.W. = 5.3% of fo
2o,p	B.W. = 4.8% of fo
3	160 decodes
4	Acceptable Amplitude Ratio (Twist) = –19.1dB to +15.2dB
5	Dynamic Range = 32.5dB
6	Guard Time = 23.3 ms
7	100% Successful decodes at N/S Ratio of – 12dBV
8	2-3 Hits Typical on Talk-Off Test

IV. APPLICATIONS

DTMF receivers have utility in systems ranging from simple push-button data communications lines to complex central telephone office applications. This section describes three basic circuits: 16-channel remote control, Tone Receiver with 2-of-8 decoded outputs, and DTMF to rotary dial pulse converter.

16-Channel Remote Control

DTMF signaling provides a simple, reliable means of transmitting information over a 2-wire twisted pair. The complete schematic of a 16-channel remote control is shown in Figure 12. When one of the key pad buttons is depressed, a tone pair is sent over the transmission medium to the SSI 201 tone receiver. The 4514 raises one of its 16 outputs in response to the 4-bit output code from the SSI 201. The output of the 4514 will remain high until the next button is depressed.

2-of-8 Output Decode

The circuit shown in Figure 13 can be used to convert the binary coded 2-of-8 output from the SSI 201 to a full 2-of-8 code (or 2-of-7 code if IN1633 is high). The output data will be valid while DV is high. If it is desired to force the eight outputs to zero when a valid tone is not present, DV should be inverted and connected to both $\overline{E}$ inputs of the 4555.

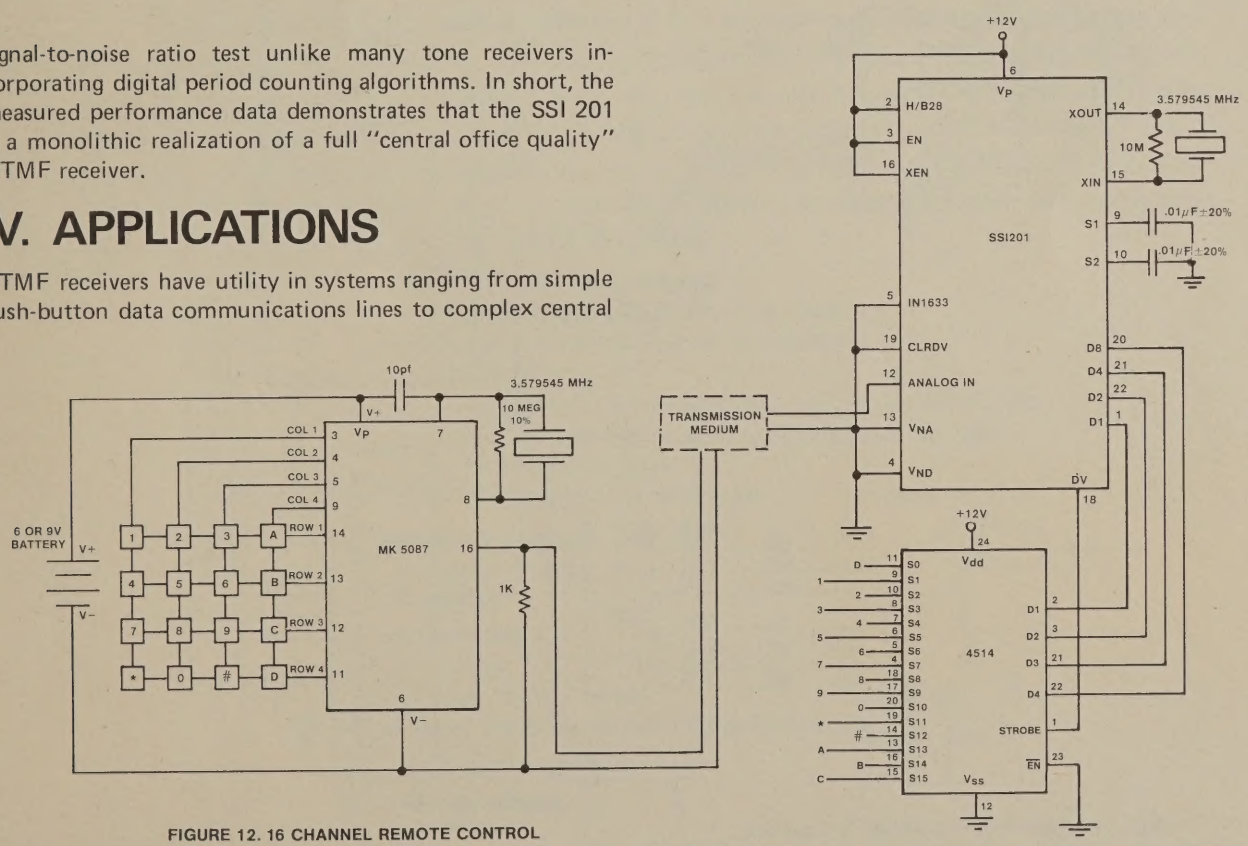

FIGURE 12. 16 CHANNEL REMOTE CONTROL

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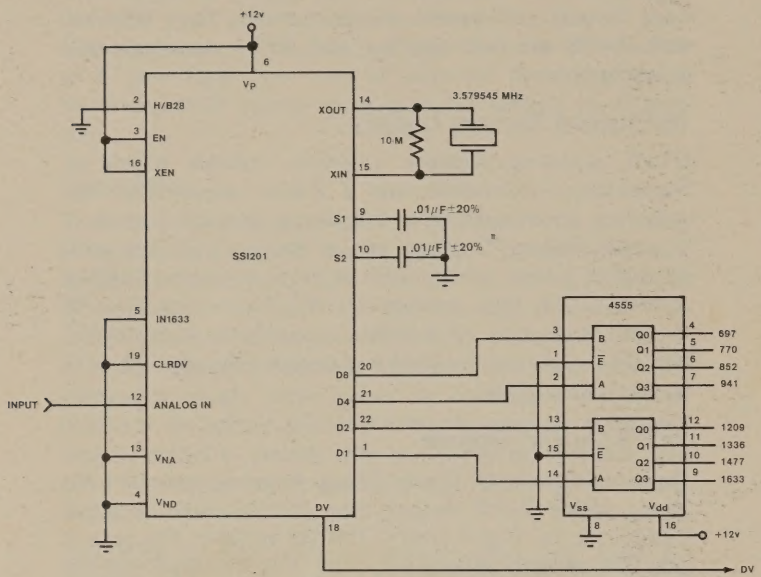

FIGURE 13. TOUCH TONE® TO 2 OF 8 OUTPUT CONVERTER.

DTMF to Rotary Dial Pulse Converter

The 2-of-8 output circuit in Figure 13 can be modified to interface with a pulse dialer as shown in Figure 14. The 4049 is used to translate the 12V outputs of the SSI 201 to the 5V swings required for the MK5099 pulse dialer.

NOTE: These specifications and descriptions are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. No responsibility is assumed by SSi for use of the SSI 201; nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. No license is granted under any patents, patent rights or trademarks of SSi. SSi reserves the right to make changes in specifications at any time and without notice.

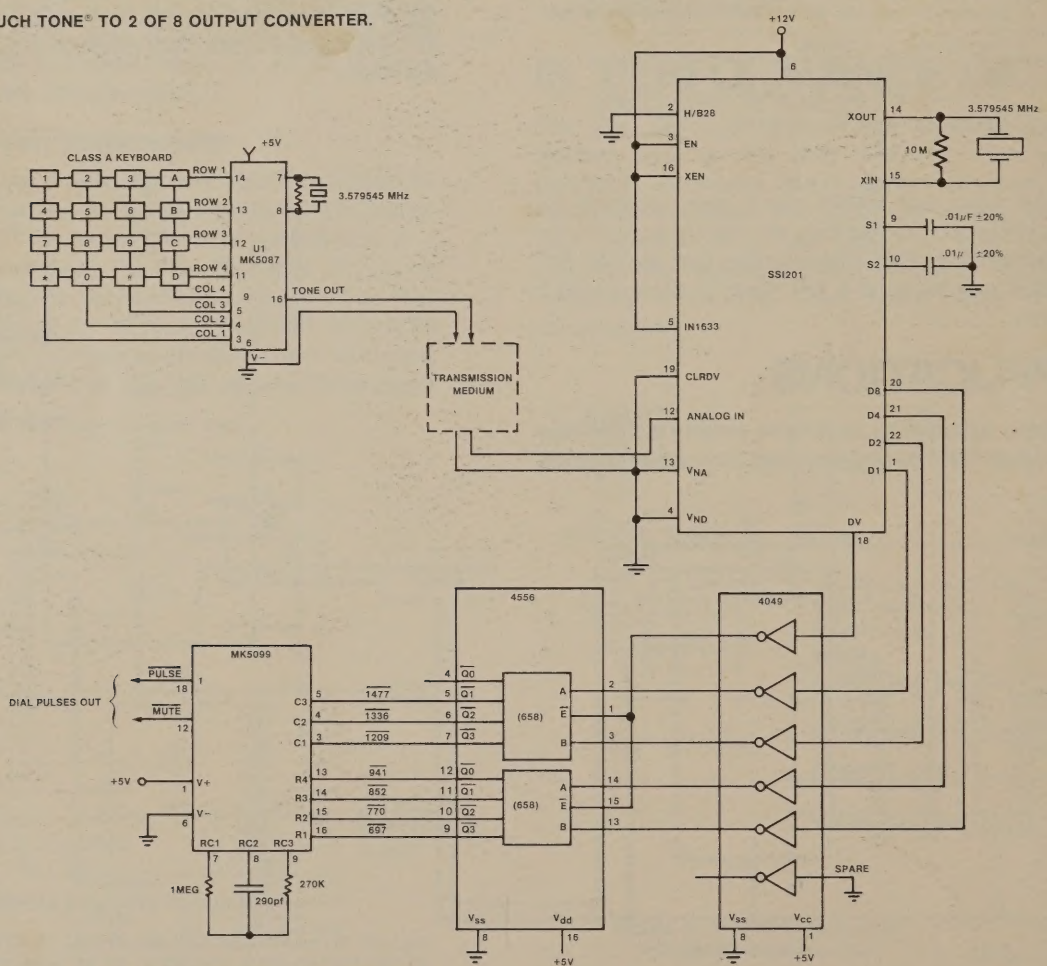

FIGURE 14. TOUCH TONE® TO ROTARY CONVERTER.

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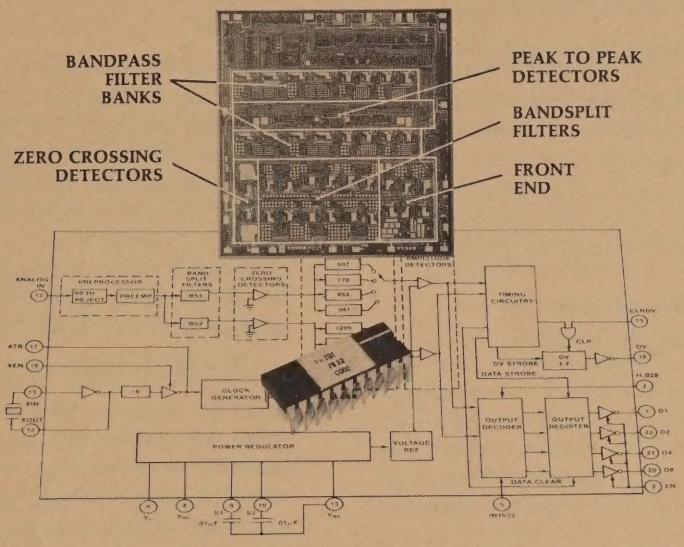
Monolithic Dual-Tone Multi-frequency Receiver Application Note



The SSI 201 Integrated DTMF Receiver is a complete Touch-Tone® detection system. It operates in a stand-alone mode for the majority of telecommunications applications, thereby providing the most economical implementation of DTMF signaling systems possible. It combines precision active filters and analog circuits with control logic on a monolithic CMOS integrated circuit. Its use is straightforward and the external component requirements are minimal. This Application Note describes the system requirements and performance of the SSI 201 DTMF Receiver.

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Application Note
SSI 201 DTMF Receiver

I. HOW THE SSI 201 WORKS

General Description of Operation

The task of a DTMF receiver is to detect the presence of a valid tone pair on a telephone line or other transmission medium. What constitutes a valid tone pair? The following table gives the established Bell system standards:

One Low-Group Tone —and— One High-Group Tone	697 or 770 or 852 or 941 Hz 1209 or 1336 or 1477 or 1633 Hz
Frequency Tolerance	$f_o \pm (1.5\% + 2Hz)$
Amplitude Range	$-24dBm \leq A \leq +6dBm$ @ 600Ω
Relative Amplitude (Twist)	$-8dB \leq \frac{\text{High-Group Tone}}{\text{Low-Group Tone}} \leq +4dB$
Duration	40ms or longer
Inter-tone Pauses	40ms or longer

The presence of a valid tone pair indicates a single dialed digit; to generate a valid digit sequence, each tone pair must be separated by a valid pause. To achieve quality data reception, the DTMF receiver must faithfully identify all valid tone pairs and not mistakenly decode other signals as tone pairs.

Figure 1 is the SSI 201 block diagram. In general terms, the detection scheme is as follows: The analog input is pre-filtered and then split into two bands, each of which contains only one DTMF tone group. The output of each band-split filter is amplified and limited by a zero-crossing detector to produce a square wave at the dominant frequency present in that filter. Thus, if the only signal at the receiver input is a valid tone pair, the output of the high-group and low-group zero-crossing detectors are square waves at a high-group tone frequency and a low-group tone frequency, respectively. A bandpass filter group is driven by each zero-crossing detector; for a valid tone pair, one of the four low-group filters and one of the four high-group filters have a high output level. By level detecting the outputs of all eight bandpass filters, proper decoding of the tone pair is achieved.

In the telephone environment, speech and noise are often present on the line with the touch tones, compounding the detection problem. The SSI 201 architecture compensates for such interference providing talk off (speech immunity) and signal to noise performance surpassing that of available digital detection circuits. The key to this superiority is the use of bandstop filters to perform the band-split function (instead of the simpler and more common bandpass filters). In combination with the zero-crossing detectors, they provide excellent talk-off characteristics. Why is this so?

The function of the zero-crossing detectors (limiters) is to produce a square wave at the prime frequency emanating from the band-split filters. If a pure tone is not present, a rectangular wave with variable period will result. This is the case for voice or noise or whenever significant interference is present with the tones. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero-crossings shift. Eventually, no single bandpass filter pair will contain significant power long enough to result in a tone detection. To be most immune to false decodes—by far the worst type of DTMF receiver error—it makes sense to eliminate as little of the incoming audio spectrum as possible ahead of the limiters. Bandpass filters reject all signals except a tone group, while the SSI 201 bandstop filters reject only one tone group, retaining

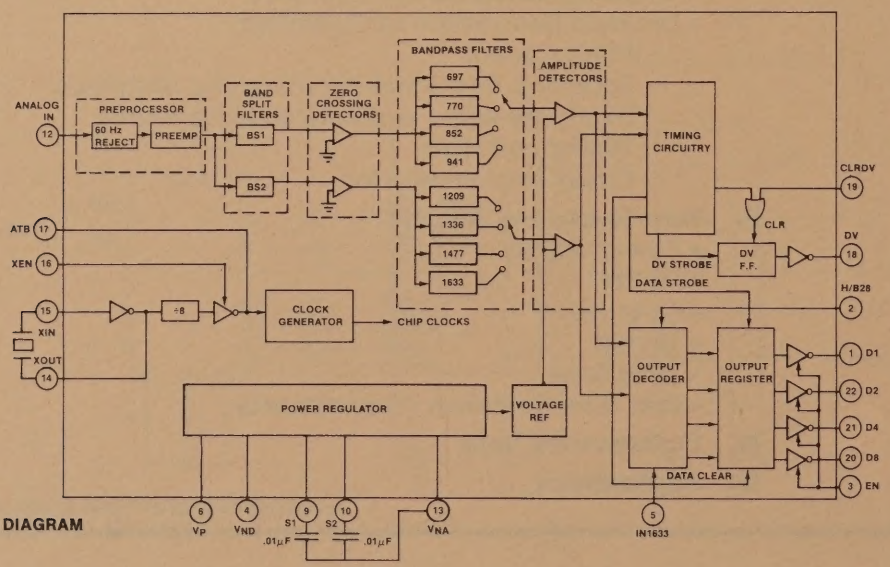


FIGURE 1. SSI 201 BLOCK DIAGRAM

the other tone group plus all other interfering audio energy. Thus it is more likely that the zero crossings will be skewed in the presence of interference with a bandstop front end than with a bandpass front end, making false tone detection far less likely.

Detailed Description of Operation

Preprocessor

The analog input first passes through the preprocessor which rejects 60 Hz and dial tone, and shapes the remaining spectrum. Dial tone and 60 Hz frequencies are attenuated to avoid filter overload which could prevent valid tone detection. In addition, the preprocessor emphasizes the higher part of the audio spectrum (typically attenuated by phone lines) to improve talk-off performance and attenuates signals above 6kHz to reduce the incoming signal to noise ratio requirement.

Bandstop Filters and Zero-Crossing Detectors

Driven by the preprocessor output, the bandstop filters separate the tone groups and drive the zero-crossing detectors. These detectors have very high gain and produce a constant amplitude output for signals above the minimum specified amplitude limits, and thus perform an AGC function. This makes detection independent of the amplitude of a valid tone pair. The SSI 201 discriminates on twist, or the relative amplitude of the two tones. This is accomplished by producing "floors" in the bandstop filters, so that a portion of the other tone group remains. Then, if the twist is too great, the zero crossings will be skewed enough by the opposite band tones to prevent detection.

Bandpass Filters and Amplitude Detectors

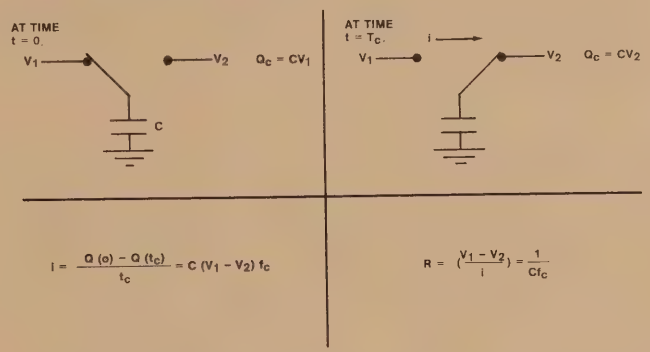
The bandpass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the filter output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuitry to ascertain the presence of one and only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

Timing and Logic

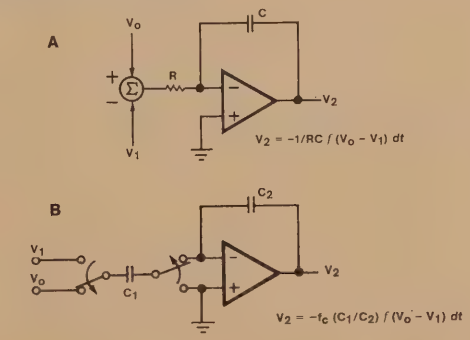
The only precision external element needed for the SSI 201 is a 3.58 MHz crystal for the on-board oscillator. This generates the precise clock for the filters and for the logical timing and controlling of the receiver. The SSI 201 is primarily analog in nature, so the logic performs bookkeeping, output formatting, and so on.

Circuit Implementation

The SSI 201 is an analog-digital system that is revolutionary in its incorporation of functions historically requiring combinations of passive and active discrete components, hybrids and digital ICs. For the first time, precision active filters with no external components or trimming requirements have been integrated with analog functional blocks and standard MOS logic. These are switched-capacitor filters* designed via classical techniques and implemented using switched capacitor resistors and integrators as shown in Figure 2. Because the filter characteristics, i.e. center frequency, Q, bandwidth and gain, are all defined by capacitor ratios, they are inherently very accurate and stable. The zero-crossing detectors and amplitude detectors are also precision analog circuits, and employ auto-zero techniques to null offsets contributed by the amplifiers and other circuitry. The logic is standard low-power, high noise immunity CMOS.



R from C. Switching a capacitor between two nodes simulates a resistor whose value depends only on the capacitor value and the switching frequency. This switched-capacitor technique allows the integration of precision filters on the DTMF chip.



Integrator. In a modification of standard integrator (**A**), C_1 of the differential switched-capacitor integrator (**B**) first charges to the difference between the two input voltages, then transfers the charge to C_2. The periodic transfer of charge appears as a current flow.

FIGURE 2. SWITCHED-CAPACITOR FILTERS

*G.M. Jacobs, G.F. Landsburg, B.J. White and D.A. Hodges, "Touch-Tone Decoder Chip Mates Analog Filters with Digital Logic," Electronics, Vol 52, No. 4, March 15, 1979, pp 105-112 (Reprints available from SSi).

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II. HOW TO USE THE SSI 201

Power Supply

The SSI 201 operates from 0°C to 70°C with a 12V ± 10% supply and typically draws 29mA. Excessive power supply noise should be avoided and to aid the user in this regard, power supply options are provided.

As with all active filter circuits, the SSI 201 is susceptible to excess power supply noise generating spurious signals at the filter outputs. In order to ensure reliable detection of -24dBm tones by the SSI 201, the wide-band power supply noise must be limited to less than 25mV peak-to-peak. Systems with higher minimum tone amplitudes will work properly with correspondingly higher power supply noise.

Since the digital circuitry of the SSI 201 possesses the high noise immunity characteristic of CMOS logic, limited power supply noise is required only for the analog supply (V_{NA}). Provision has been made on the SSI 201 to separate the analog (V_{NA}) and digital (V_{ND}) supplies, permitting an unfiltered supply to be used at V_{ND}. It is necessary however that:

$$V_{ND} < V_{NA} + .5 \text{ volts}$$

Power supply noise effects will be slightly less if the analog input is referenced to V_P. This is normally accomplished by connecting V_P to system ground and providing negative voltages for V_{NA} and V_{ND}. The power supply noise limit, however, is sufficient to ensure operation when the analog input is referenced to either V_P or V_{NA}.

Inputs

The SSI 201 contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit. A destructive high current mode may occur if input or output voltages are not constrained to the range between V_P and V_{ND}.

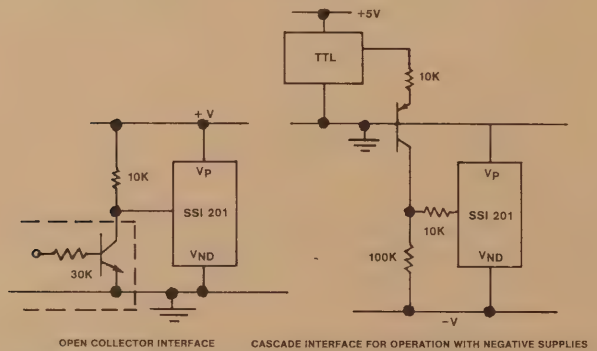


FIGURE 3. INTERFACE CIRCUITS FOR CONVERSION FROM TTL OUTPUT LEVELS TO SSI 201 INPUT LEVELS.

The digital inputs (H/B28, EN, IN1633, XEN and CLRDV) are directly compatible with standard CMOS logic parts powered by V_P and V_{ND}. Each input presents an impedance of greater than $10^9\Omega$ to incoming signals. To guarantee logic levels, inputs should swing to within 30% of V_P or V_{ND}. If it is desired to control the SSI 201 with TTL, the interface circuits shown in Figure 3 may be used.

The ANALOG IN input is the signal input pin to the SSI 201 receiver, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 4. The signal level at the ANALOG IN pin must neither exceed the positive supply nor fall more than 22V below it. If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a .01μF ± 20% capacitor. The internal bias resistor is greater than 100kΩ.

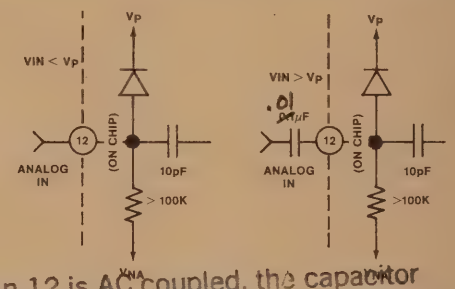


FIGURE 4. DIRECT AND AC COUPLED INPUT CONFIGURATIONS

The SSI 201 will tolerate total input rms noise up to 12dB below the lowest amplitude tone. For most telephony applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the SSI 201 unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter of Figure 5 may be employed to band limit the incoming signal.

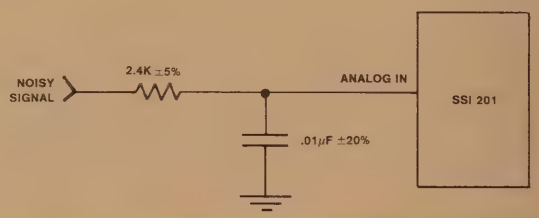


FIGURE 5. FILTER FOR USE IN EXTREME HIGH FREQUENCY INPUT NOISE ENVIRONMENT.

The S1 and S2 pins are connected to a portion of the zero-crossing detector circuitry. These pins should be bypassed to system ground with at least 0.01μF ± 20% capacitors.

Outputs

The digital outputs of the SSI 201 (D1, D2, D4, D8, DV, ATB) swing between V_P and V_{ND} and are fully compatible with standard CMOS logic parts powered from V_P and V_{ND}. The I-V characteristic of the digital outputs is plotted in Figure 6.

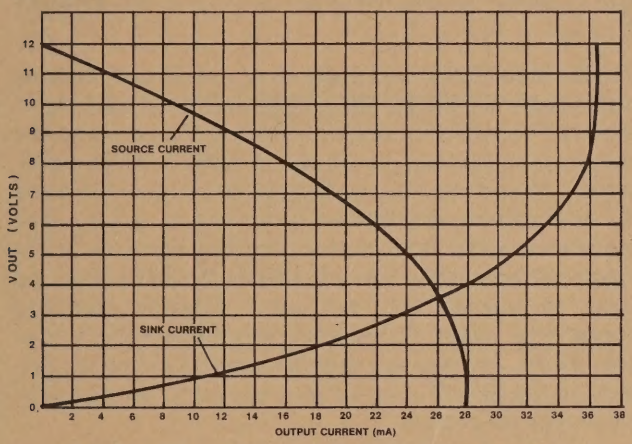


FIGURE 6. SSI 201 TYPICAL DATA OUTPUT ($V_P - V_{ND}$ = 12.0v)

A standard CMOS 4049B or 4050B can be used as shown in Figure 7 to interface the SSI 201 to TTL or low voltage MOS.

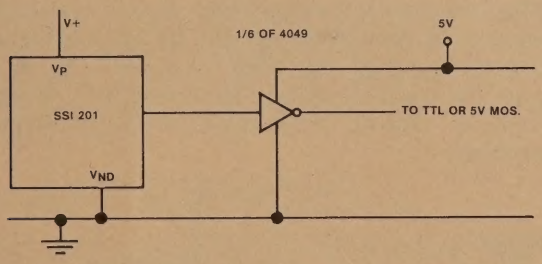


FIGURE 7. SSI 201 TO TTL OR LOW VOLTAGE MOS INTERFACE.

The data outputs (D1, D2, D4, D8) are three-state enabled to facilitate interface to a three-state bus. Figure 8 shows the equivalent circuit for the data outputs in the high impedance state. Care must be taken to prevent either diode in Figure 8 from becoming forward biased.

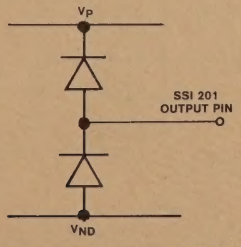
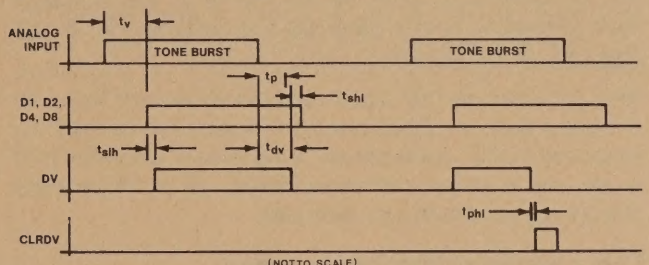


FIGURE 8. EQUIVALENT CIRCUIT OF SSI 201 DATA OUTPUT IN HIGH IMPEDANCE STATE

Timing

A timing diagram illustrating receiver operation is shown in Figure 9. Within 40ms of a valid tone pair appearing at the SSI 201 receiver input, the data outputs (D1, D2, D4, and D8) will become valid. Seven microseconds after the data outputs have become valid, DV will be raised. The data outputs will remain valid and DV will remain high as long as a valid tone pair is present at the receiver input. Within 40ms of the removal of a valid tone pair from the input, the SSI 201 will recognize a valid pause. DV is lowered approximately 45ms after the tone pair is removed. The data outputs will be cleared (all set to zero) 4.4ms after DV is lowered. The SSI 201 timing guarantees that the DV strobe will be of at least the same duration as the incoming tone pair. Figure 9 also lists the propagation delay specifications for the digital outputs of the SSI 201.



KEY

SYMBOL	DEFINITION	SPEC MIN	SPEC TYP	SPEC MAX	UNIT	CONDITION (V_P - (V_{NA} = V_{ND}) = 12V ±10% TA = 0°C-70°C
t_v	TONE DETECTION TIME	20	--	40	ms	--
t_{slh}	DATA OVERLAP OF DV RISING EDGE	7	--	--	µs	CLRDV = V_{ND}, EN = V_P
t_p	PAUSE DETECTION TIME	25	--	40	ms	--
t_{dv}	TIME BETWEEN END OF TONE AND FALL OF DV	40	45	50	ms	--
t_{shl}	DATA OVERLAP OF DV FALLING EDGE	4	--	4.4	ms	--
t_{phl}	PROP. DELAY: RISE OF CLRDV TO FALL OF DV MEASURED AT 50% POINTS	--	--	1	µs	CI = 300 pF
---	OUTPUT ENABLE TIME: MEASURED FROM 50% POINT OF RISING EDGE OF EN TO THE 50% POINT OF THE DATA OUTPUT WITH RI TO OPPOSITE RAIL	--	--	1	µs	CI = 300pF, RI = 10K
---	OUTPUT DISABLE TIME: MEASURED FROM 50% POINT OF FALLING EDGE OF EN TO TIME AT WHICH OUTPUT HAS CHANGED 1V WITH RI TO OPPOSITE RAIL	--	--	1	µs	CI = 300pF, RI = 1K ΔV = 1V
---	OUTPUT 10-90% TRANSITION TIME	--	--	1	µs	CI = 300pF.

FIGURE 9. TIMING DIAGRAM AND SPECIFICATIONS.

Provision has been made on the SSI 201 for handshake interface with an outside monitoring system. In this mode, the DV strobe is polled by the monitoring system at least once every 40ms to determine whether a new valid tone pair has been detected. If DV is high indicating that a new valid tone pair has been detected, the monitoring system stores the coded data present at the data outputs of the receiver and clears DV by pulsing CLRDV high. With some systems operating in the handshake mode, it may be desirable to know when the valid tone has ended. Ordinarily this would be indicated by the falling edge of DV. However, in the handshake mode, DV is cleared by the monitoring system each time a new valid tone is detected and, therefore, cannot be used to determine when a valid tone pair has ended. The termination of a valid tone pair in this case may be observed by detecting the clearing of the data outputs. Since, in hexidecimal format (the mode

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normally used with a handshake interface), the all zero state represents a commonly unused tone pair (D), the end of a valid tone pair may be detected by connecting a four-input NOR gate to the outputs and sensing the all zero state.

Time Base

The SSI 201 contains an on-chip oscillator for a 3.579545 MHz parallel resonant quartz crystal. The CTS Part No. MP036 or Workman Part No. CY1-C or equivalent is recommended for use with the SSI 201 oscillator. The crystal is connected between XIN and XOUT, while XEN is tied high. In this mode, the ATB (alternate time base) pin delivers a square wave output at one-eighth the crystal oscillator frequency (447.443 kHz). A capacitor (C≅10pF) may be added in parallel with the crystal to trim the oscillator frequency, but is generally not required for proper operation of the SSI 201.

The ATB pin can be converted to a time base input by removing the crystal and tying XIN and XEN high and low respectively. By driving these ATB inputs with the ATB output of a crystal connected device, up to 25 receivers may be operated with a single crystal.

Dial Tone Rejection Requirements

The SSI 201 tolerates precise dial tone (350 Hz and 440 Hz at equal amplitudes) up to 0 dB relative to the lowest Touch-Tone® level*—adequate for most applications. In a high dial tone environment, the filter of Figure 10 may be used. This filter exhibits an elliptic highpass response that provides a minimum of 18 dB rejection at 350 Hz and 24 dB rejection at 440 Hz so long as the component tolerances indicated are observed. The SSI 201 on-chip filters reject 350 Hz at least 6 dB more than 440 Hz. Therefore, employing the filter of Figure 10 yields a dial tone tolerance of +24 dB. In a system where -24 dBm Touch-Tones® are present, the SSI 201 used in conjunction with the filter of Figure 10 will operate correctly in the presence of a 0 dBm dial tone (-3 dBm per dial tone frequency). The filter of Figure 10 also rejects 60 Hz by approximately 30 dB.

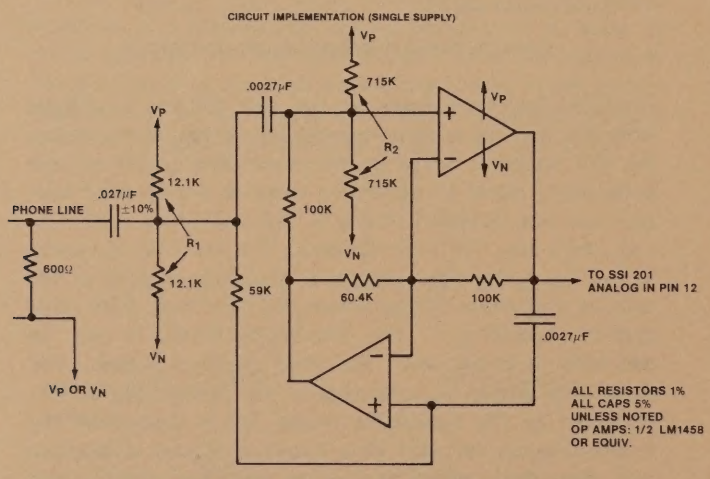

FIGURE 10. DIAL TONE REJECT FILTER.

*For dial tones of different amplitudes, the total power of the two dial tone frequencies must be no more than 0 dB relative to the lowest amplitude Touch-Tone.

The dial tone filter circuit is shown operated from the same single supply as the SSI 201 necessitating the splitting of resistors R_1 and R_2 for proper biasing of the op amps. If a dual polarity supply is available to power the op amps, resistors R_1 and R_2 may be replaced with single 5.9 kΩ and 357 kΩ resistors, respectively, connected to ground. It is recommended that the dial tone filter be powered from the highest voltage supply available (within the limits of the op amps) to provide the large signal handling capability necessary to accept Touch-Tones® in the presence of dial tone, 60 Hz, and any interference. Input coupling requirements to the SSI 201 must be observed as mentioned earlier in this application note.

III. PERFORMANCE DATA

The SSI 201 tone receiver has been subjected to the rigorous tests on the Mitel CM7290 tone receiver test cassette. This cassette checks receiver detection bandwidth, maximum acceptable amplitude ratio (twist), receiver guard time, dynamic range and signal to noise ratio. It also evaluates the receiver's speech immunity (talk-off) with a recording of excerpts from many hours of telephone conversations.

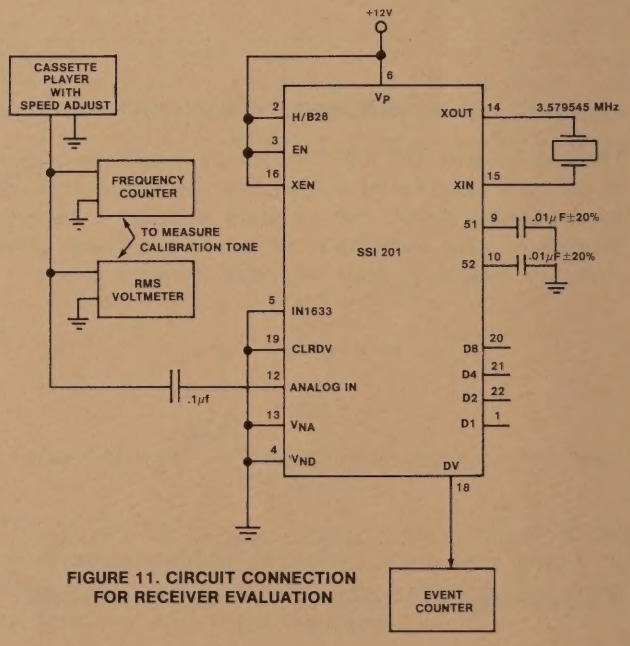

FIGURE 11. CIRCUIT CONNECTION FOR RECEIVER EVALUATION

The evaluation circuit shown in Figure 11 was used to characterize the SSI 201. The speed and output level of the tape deck must be adjusted so that the calibration tone at the beginning of the tape is at exactly 1000Hz and 2V rms.

Test results for the SSI 201 are summarized in Table I. The SSI 201 registers only two "hits" on the talk-off test-performance as good as the best receivers currently available. The SSI 201 detects all 1000 pulses in the 12 dB signal-to-noise ratio test unlike many tone receivers incorporating digital period counting algorithms. In short, the measured performance data demonstrates that the SSI 201 is a monolithic realization of a full "central office quality" DTMF receiver.

TABLE I
MITEL #CM7290 TAPE TEST RESULTS:
(Averaged for 10 parts)

TEST #	RESULTS
2a,b	B.W. = 5.0% of fo
2c,d	B.W. = 5.0% of fo
2e,f	B.W. = 5.3% of fo
2g,h	B.W. = 4.9% of fo
2i,j	B.W. = 5.0% of fo
2k,l	B.W. = 5.3% of fo
2m,n	B.W. = 5.3% of fo
2o,p	B.W. = 4.8% of fo
3	160 decodes
4	Acceptable Amplitude Ratio= – 19.1dB to +15.2dB
5	Dynamic Range = 32.5dB
6	Guard Time = 23.3 ms
7	100% Successful decodes at N/S Ratio of – 12dBV
8	2-3 Hits Typical on Talk-Off Test

IV. APPLICATIONS

DTMF receivers have utility in systems ranging from simple push-button data communications lines to complex central telephone office applications. This section describes three basic circuits: 16-channel remote control, Tone Receiver with 2-of-8 decoded outputs, and DTMF to rotary dial pulse converter.

16-Channel Remote Control

DTMF signaling provides a simple, reliable means of transmitting information over a 2-wire twisted pair. The complete schematic of a 16-channel remote control is shown in Figure 12. When one of the key pad buttons is depressed, a tone pair is sent over the transmission medium to the SSI 201 tone receiver. The 4514 raises one of its 16 outputs in response to the 4-bit output code from the SSI 201. The output of the 4514 will remain high until the next button is depressed.

2-of-8 Output Decode

The circuit shown in Figure 13 can be used to convert the binary coded 2-of-8 output from the SSI 201 to a full 2-of-8 code (or 2-of-7 code if IN1633 is high). The output data will be valid while DV is high. If it is desired to force the eight outputs to zero when a valid tone is not present, DV should be inverted and connected to both $\overline{E}$ inputs of the 4555.

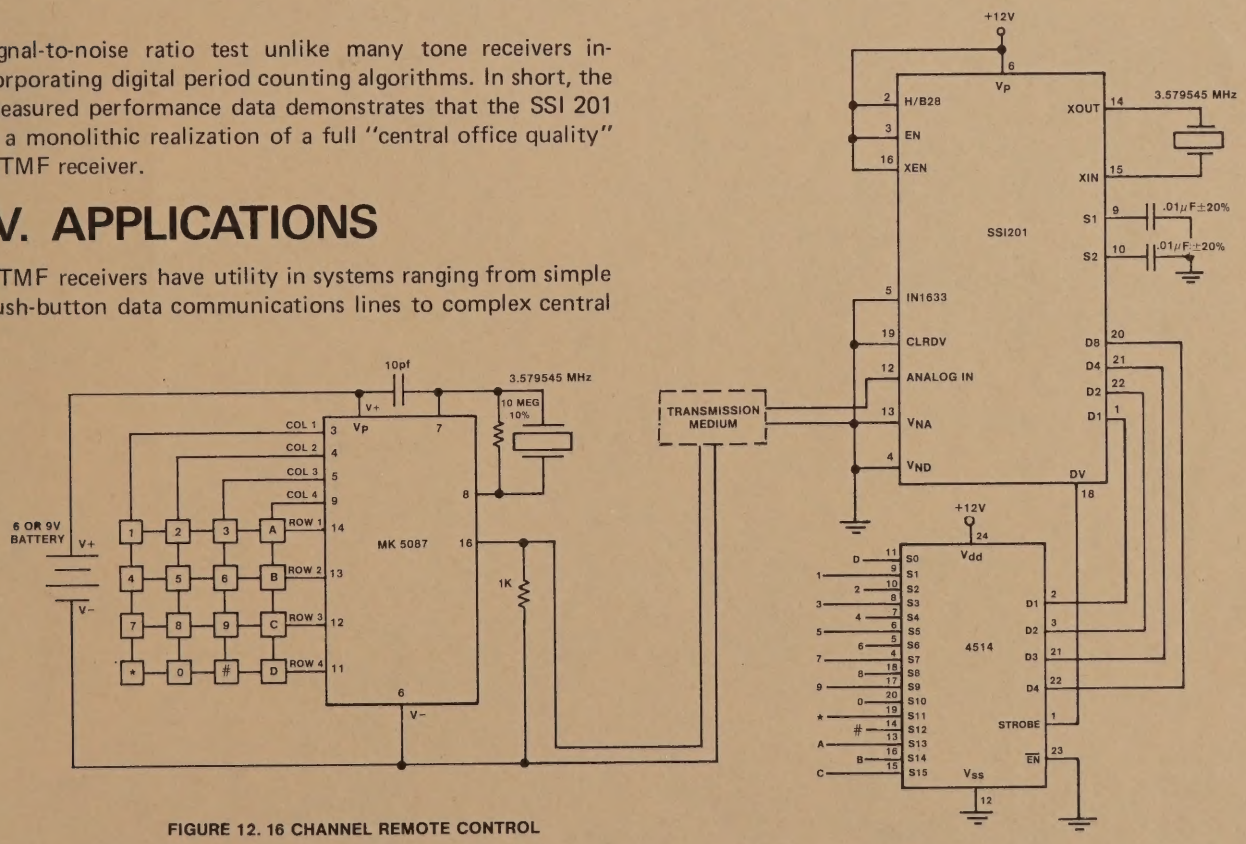

FIGURE 12. 16 CHANNEL REMOTE CONTROL

Silicon Systems
incorporated
14351 Myford Road • Tustin, CA 92680 • (714) 731-7110 • TWX 910-595-2809

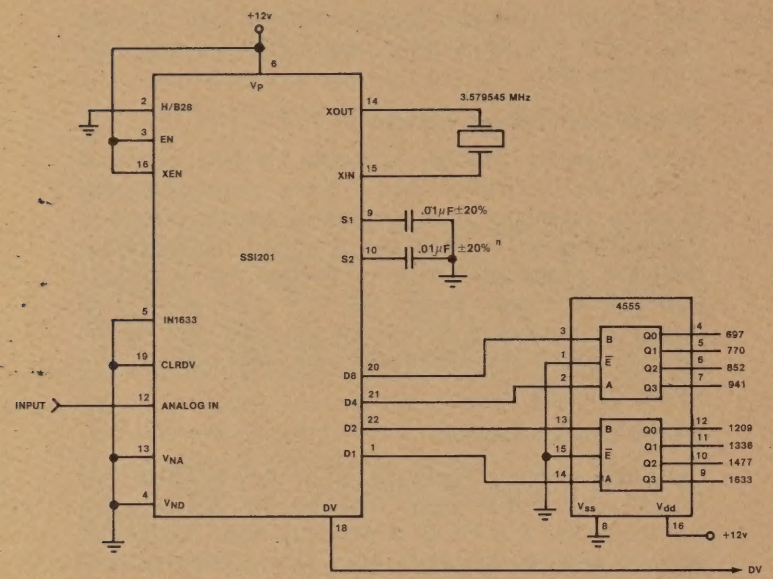

FIGURE 13. TOUCH TONE® TO 2 OF 8 OUTPUT CONVERTER.

DTMF to Rotary Dial Pulse Converter

The 2-of-8 output circuit in Figure 13 can be modified to interface with a pulse dialer as shown in Figure 14. The 4049 is used to translate the 12V outputs of the SSI 201 to the 5V swings required for the MK5099 pulse dialer.

NOTE: These specifications and descriptions are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. No responsibility is assumed by SSi for use of the SSI 201; nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. No license is granted under any patents, patent rights or trademarks of SSi. SSi reserves the right to make changes in specifications at any time and without notice.

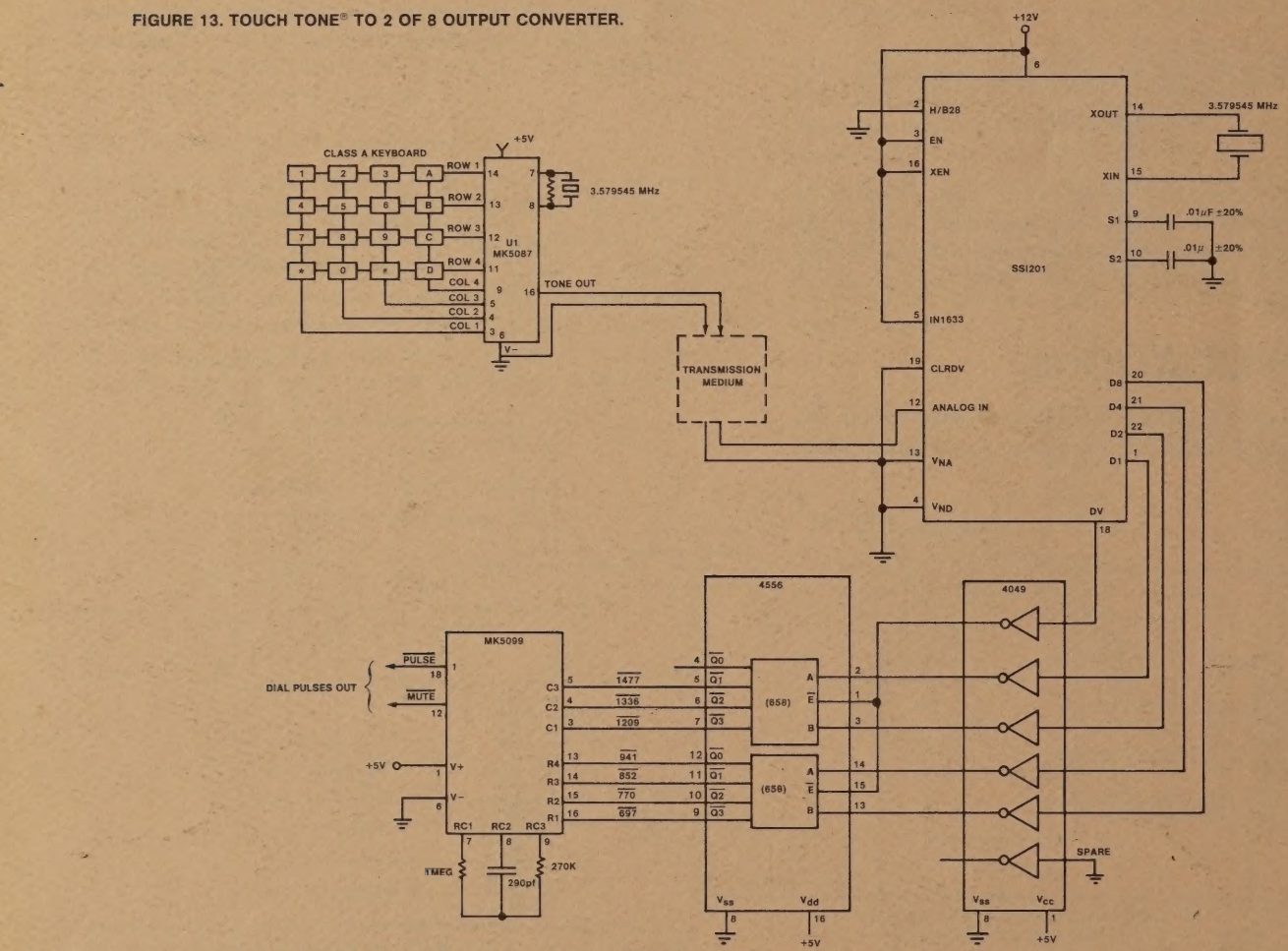

FIGURE 14. TOUCH TONE® TO ROTARY CONVERTER.